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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/773,283	02/09/2004	Masataka Sasaki	62807-160	3488

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EXAMINER	
KITOV, ZEEV	

ART UNIT	PAPER NUMBER
2836	

DATE MAILED: 04/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/773,283	SASAKI ET AL.
	Examiner	Art Unit
	Zeev Kitov	2836

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 - 13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 - 13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 February 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *02/09/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

1. Claims 1 and 11 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter, which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. A reason for that is in the following claim limitation: "a second comparator which detects a gate voltage of said power management semiconductor device to output a second detection signal, when the detected gate signal exceeds a second reference voltage which is a minimum gate voltage for feeding a rated power to said power management semiconductor device or over, and less than a line power voltage of a drive circuit for outputting a drive signal that drives said power management semiconductor device;" (emphasis added). In the circuit illustrated in Fig.1 and thoroughly described in Specification (page 7, line 3 – page 8, line 15) the second detector can detect an event that the gate voltage exceeds a second reference voltage (by issuing the logic "0" signal at the output) but unable to detect an event that the gate

voltage exceeds the power line voltage since the second detector has no means to distinguish between too high voltage and the voltage higher than the reference voltage.

For purpose of examination, the recited limitation was not given patentable weight.

2. Claims 1 and 11 are further rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter, which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. A reason for that is in the following claim limitation: "logic means for outputting a protection start signal when both the first and second detection signals are being outputted; and gate voltage reduction means for reducing said gate voltage in accordance with the protection start signal from said logic means" (emphasis added). In a case of both the collector voltage and the gate voltage exceeding their references the first and the second comparators issue the logic "0" signals. The logic AND circuit is not intended to detect such event. It issues logic "0" signal if only one of its inputs has logic "0". Therefore presence of two such signals (logic "0"s) in the inputs of the AND gate is a wrong condition to indicate a coincident presence of proper collector and gate voltages. For purpose of examination, the AND gate in the Drawing and Specification was ignored. It was assumed that some unknown logic means performs the disclosed function.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter, which the applicant regards as his invention.

3. Claims 5 – 8 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. A reason for that is in following limitation: "the first reference voltage of said comparator is a collector voltage during the time when said power management semiconductor device is electrically continuous, or over..." (emphasis added). A meaning of this limitation is obscure, since it is not clear how the device can be electrically continuous, or over (?) Specification does not provide any explanation; it just repeats the same phrase (page 4, line 25 – page 5, line1). For purpose of examination it was assumed that the first reference voltage of said comparator is a collector voltage lower that the power voltage of the drive circuit.

Drawings

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the elements of Claims 1 and 11 identiified above (see rejection under USC 112, 1st paragraph) must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure

is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

Specification is objected to due to a reasons identified in USC 112, 1st paragraph rejection of Claims 1 and 11 (see above). The Specification (page 7, line 3 – page 8, line 15) discloses the circuit, which cannot operate according to limitations of Claims 1 and 11. Appropriate corrections are required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1 - 4 are rejected under 35 U.S.C. 102(b) as being anticipated by Kimura et al. (US 5,210,479). Regarding Claim 1, Kimura et al. disclose all the elements of the claim including: a first comparator (elements 12, 13, 15, 23, 3 and 5 in Fig. 8), which detects a collector voltage of the power management semiconductor device and outputs a fist detection signal (base voltage of transistor 15 in Fig. 8) when the detected collector voltage exceeds a first reference voltage (voltage drop across element 14 in Fig. 8); a second comparator (element 31 in Fig. 8) which detects a gate voltage of the power management semiconductor device to output a second detection signal (collector current of transistor 31 in Fig. 8), when the detected gate signal exceeds a second reference voltage (Vgo), which is a minimum gate voltage for feeding a rated power to said power management semiconductor device or over; logic equivalent means for outputting a protection start signal (collector current of transistor 15 in Fig. 8) when both the first and second detection signals are being outputted; and gate voltage reduction equivalent means (elements 16, 17, 18 and 6 in Fig. 8) reducing the gate voltage in accordance with the protection start signal from the logic means (col. 10, lines 7 – 55).

Regarding Claim 2, Kimura et al. disclose the second comparator detecting the gate voltage based on a voltage separated by a separation resistance (elements 9, 11 and 32 in Fig. 8) separating a gate voltage of the power management semiconductor device.

Regarding Claims 3 and 4, Kimura et al. disclose the equivalent gate voltage reduction means (elements 15, 16, 17, 18, 6 7 and 8 in Fig. 8) cutting off a drive signal of the drive circuit and reducing the gate voltage (col. 10, lines 7 – 55).

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 5 – 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kimura in view of Horowitz et al. textbook, The Art of Electronics. As was stated above, Kimura et al. disclose all the elements of Claims 1 – 4. However, regarding Clams 5 – 8, they do not disclose the first reference voltage as being lower than the line power voltage. Horowitz et al textbook demonstrate that the collector voltage may go beyond the power supply voltage due to inductive load reaction (pages 52 – 53). However, according to them, it may cause breakdown of the switching transistor. Therefore, the switching transistor is to be protected against voltages exceeding the normal power supply value. Therefore, the first reference voltage used to detect departure of the collector voltage from normal predetermined value in the Kimura et al. circuit must be lower than the line power voltage. Both references have the same problem solving area, namely protecting the power switching transistors. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the Kimura et al. solution by setting the first reference voltage lower than the line power voltage, because otherwise the protection circuit of Kimura et al. will become useless.

Claims 9 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kimura et al. Claims 9 and 10 differ from Claims 1 and 2 rejected accordingly by their limitation of both comparators, logic means and gate voltage reduction means and drive circuit being integrated into a single semiconductor integrated circuit. Examiner takes an Official Notice, that today it is common practice in the electronic industry to integrate semiconductor circuits into a common package, i.e. integrated circuit. A particular reference will be provided upon request. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the Kimura et al. solution by integrating all the parts of the circuit, except the IGBT, into a single integrated package, because it will reduce the cost, increase the reliability and improve the environmental protection of the circuit.

Claims 11 – 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wacknov et al. (US 6,812,586) in view of Kimura et al. Wacknov et al. disclose following elements of the claim: the converter including a power semiconductor device for converting DC current to AC current (element 374 in Fig. 10); a power management semiconductor device (inherent in the structure of the load converter 374 in Fig. 10), which controls a switching operation of said power semiconductor device (elements 514 in Fig. 10). However, it does not disclose the protection circuit for power semiconductor devices. Kimura et al. disclose the protection circuit for power semiconductor devices including: a first comparator (elements 12, 13, 15, 23, 3 and 5 in Fig. 8), which detects a

collector voltage of the power management semiconductor device and outputs a fist detection signal (base voltage of transistor 15 in Fig. 8) when the detected collector voltage exceeds a first reference voltage (voltage drop across element 14 in Fig. 8); a second comparator (element 31 in Fig. 8) which detects a gate voltage of the power management semiconductor device to output a second detection signal (collector current of transistor 31 in Fig. 8), when the detected gate signal exceeds a second reference voltage (Vgo), which is a minimum gate voltage for feeding a rated power to said power management semiconductor device or over; logic equivalent means for outputting a protection start signal (collector current of transistor 15 in Fig. 8) when both the first and second detection signals are being outputted; and gate voltage reduction equivalent means (elements 16, 17, 18 and 6 in Fig. 8) reducing the gate voltage in accordance with the protection start signal from the logic means (col. 10, lines 7 – 55). Both references have the same problem solving area, namely driving the load by power transistors. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the Wacknov et al. solution by adding the protection circuit for power semiconductor devices according to Kimura et al. because, as Kimura et al. state (col. 1, lines 31 – 48), the IGBT are especially vulnerable to the short circuit conditions, and therefore should have special protection against that.

Regarding Claims 12 and 13, Wacknov et al. disclose a hybrid electric vehicle having an internal combustion engine (element 70mn in Fig. 21), an electric motor (element 534 in Fig. 11), a transmission transmitting power from the internal combustion

engine and/or the electric motor to wheels, which is inherent in the structure of the hybrid electric vehicle, an inverter unit (element 374 in Fig. 10) converting DC power to AC power, and a DC power storage unit (element 364 in Fig. 6), wherein the electric motor (element 10 in Fig. 2) is an AC motor driven by AC power from the inverter unit (col. 12, lines 30 – 14). As to the inverter unit being the power converter protected against short circuit, Kimura et al. disclose that subject (see Claim 11 rejection above).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Zeev Kitov whose current telephone number is (571) 272 - 2052. The examiner can normally be reached on 8:00 – 4:30. If attempts to reach examiner by telephone are unsuccessful, the examiner's supervisor, Brian Sircus can be reached on (571) 272 – 2800, Ext. 36. The fax phone number for organization where this application or proceedings is assigned is (703) 872-9306 for all communications.

Z.K.
04/08/2005

Stephen W. Jackson
4.8.05

STEPHEN W. JACKSON
PRIMARY EXAMINER